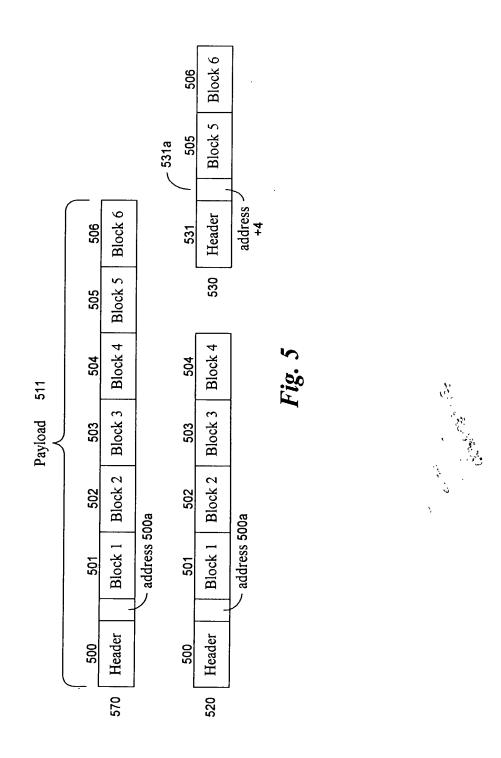
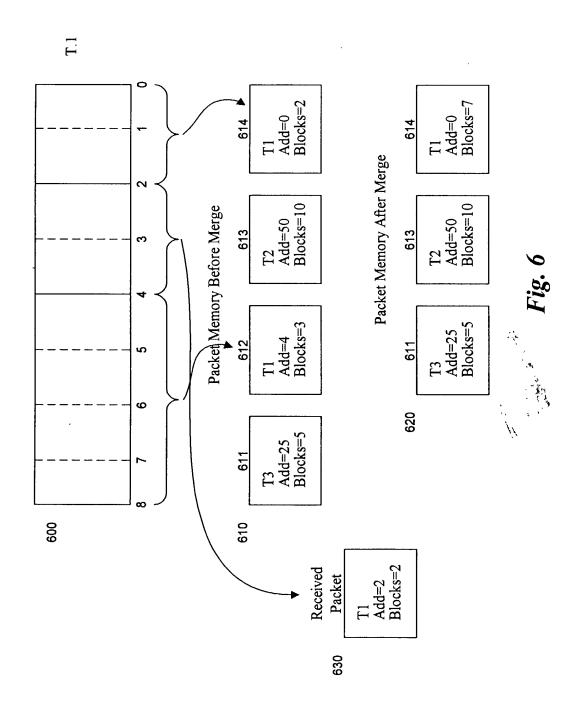


Fig. 4







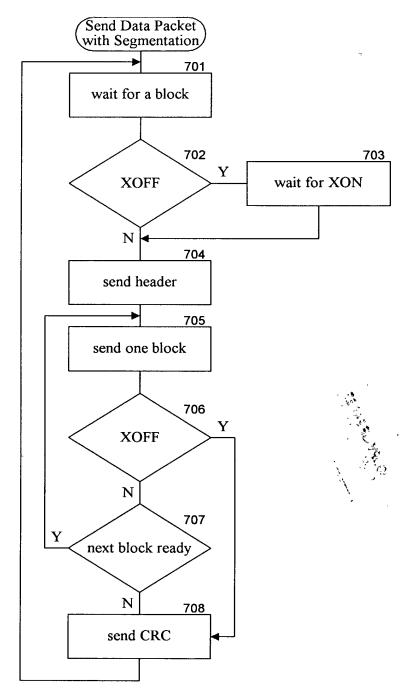


Fig. 7

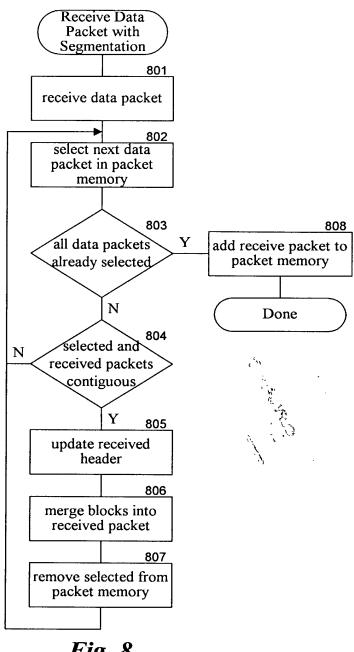
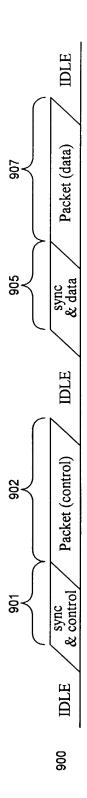


Fig. 8



sync & packet type

Fig. 9A

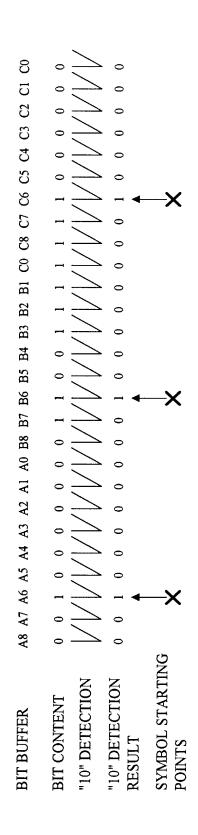
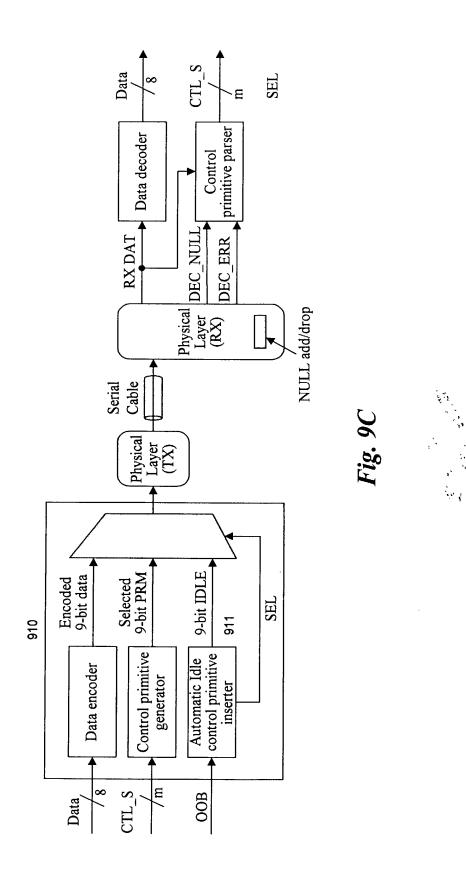
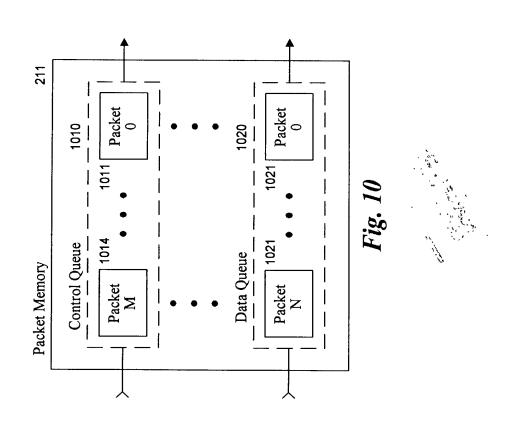
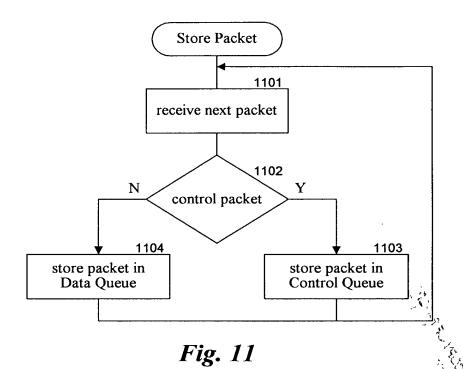


Fig. 91







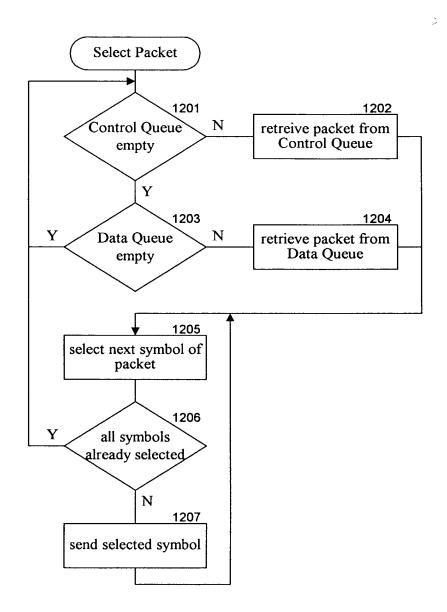
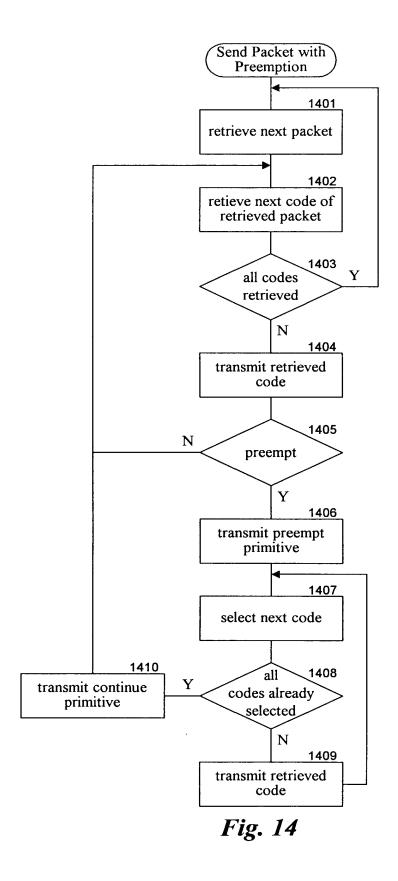


Fig. 12

	IDLE	
1305	data	packet (cont'd)
1304	continue	
1303	control	packet
1302	Preempt	
1301	data	/ packet /
	1	IDLE
	1300	

Fig. 13



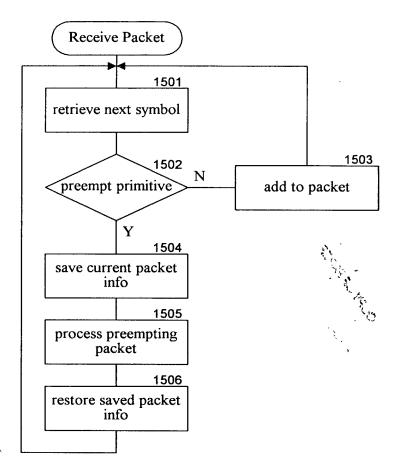
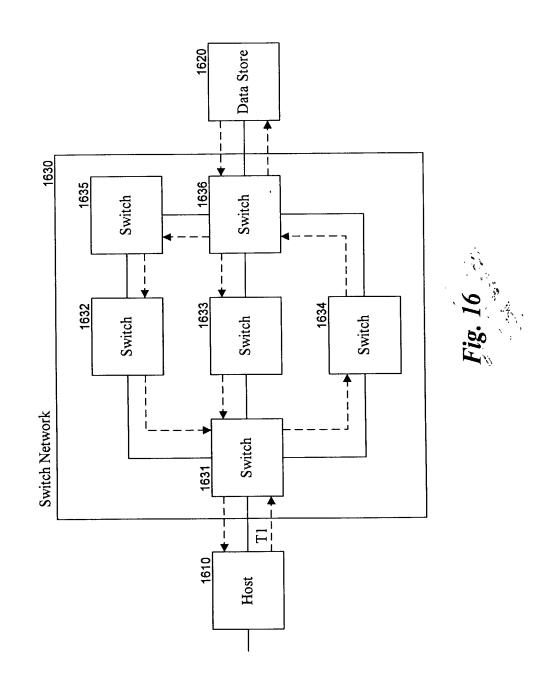
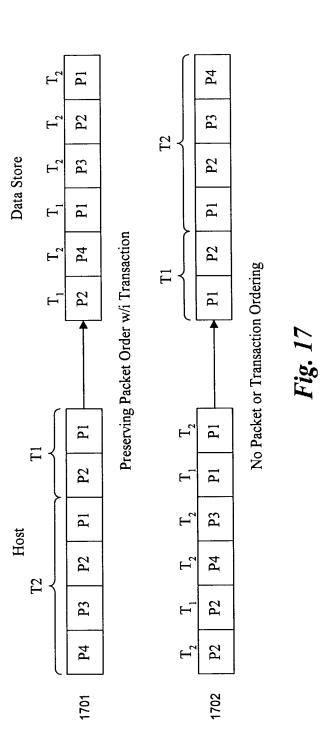


Fig. 15





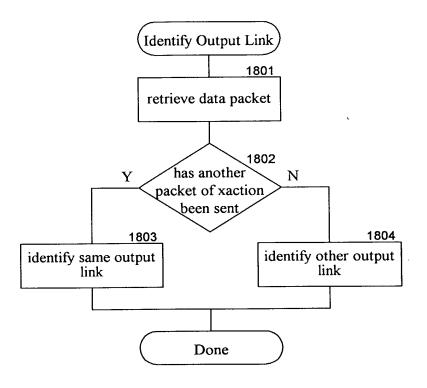
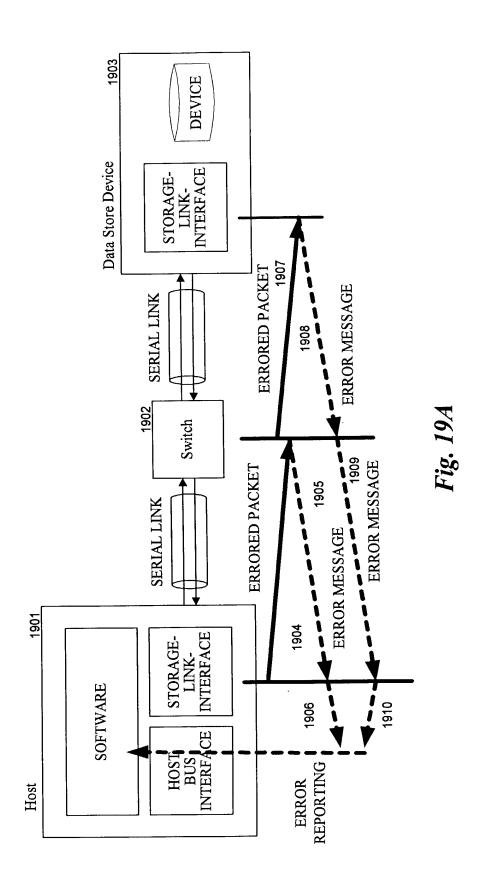
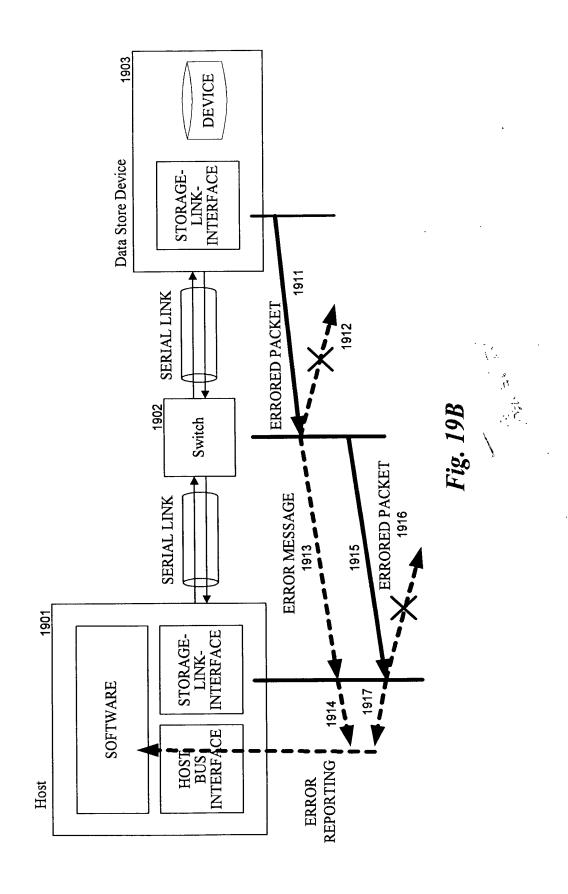


Fig. 18





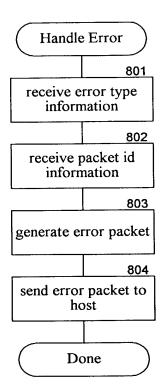
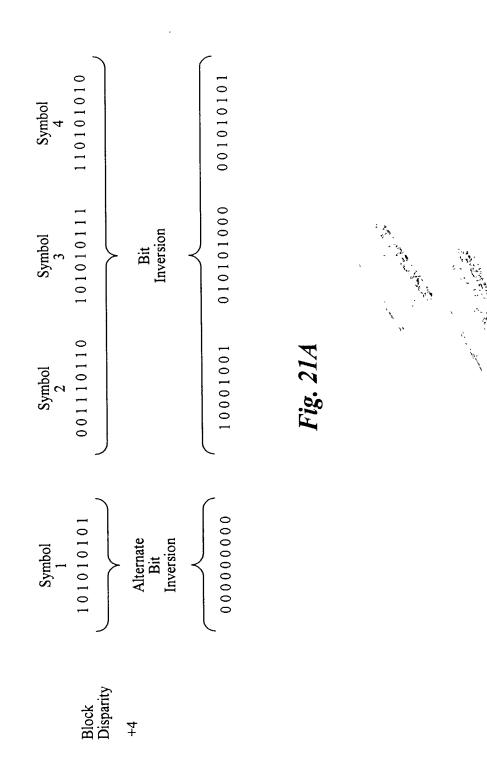
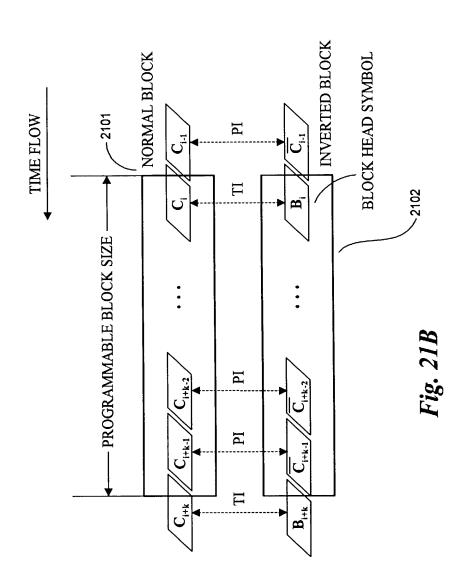


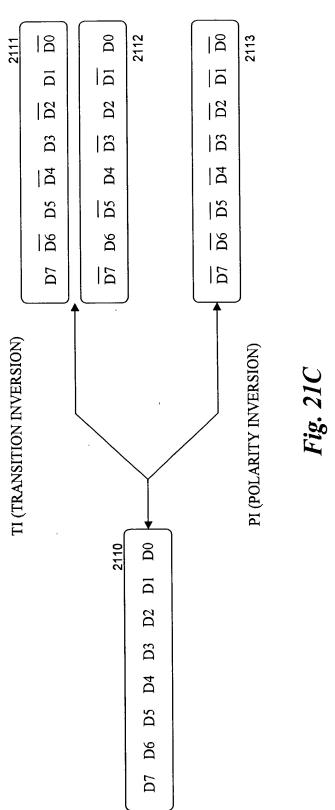
Fig. 19C

8b code	9 bit symbol	
0000 0000	101010101	
0000 0001	101010100	
0000 0010	101010111	
0101 0101	001010101	
0111 0110	001110110	
0111 0111	100100010	
1111 1111	110101010	

Fig. 20







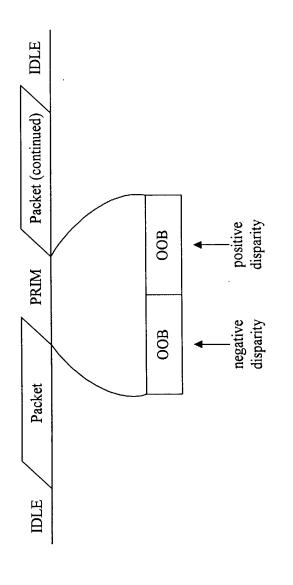


Fig. 22

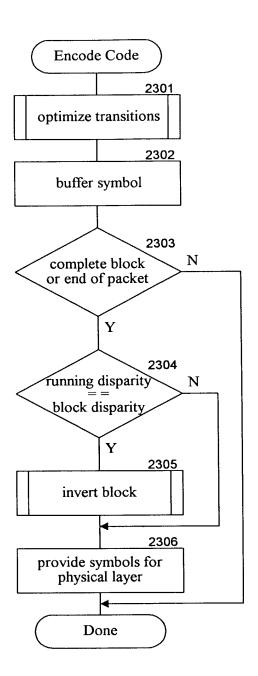


Fig. 23

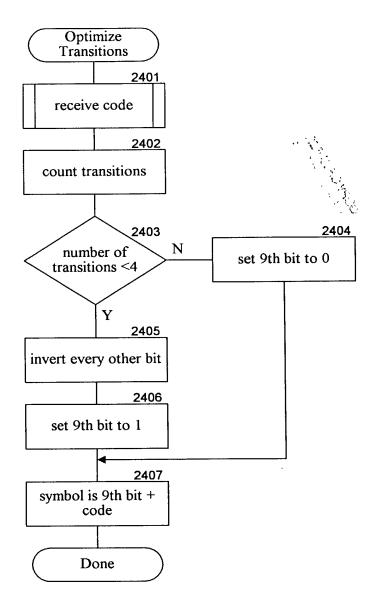


Fig. 24

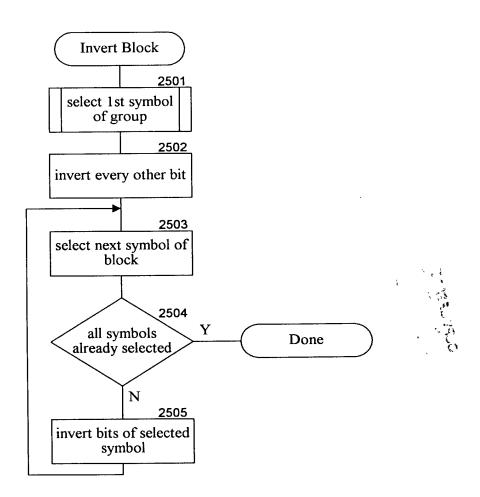
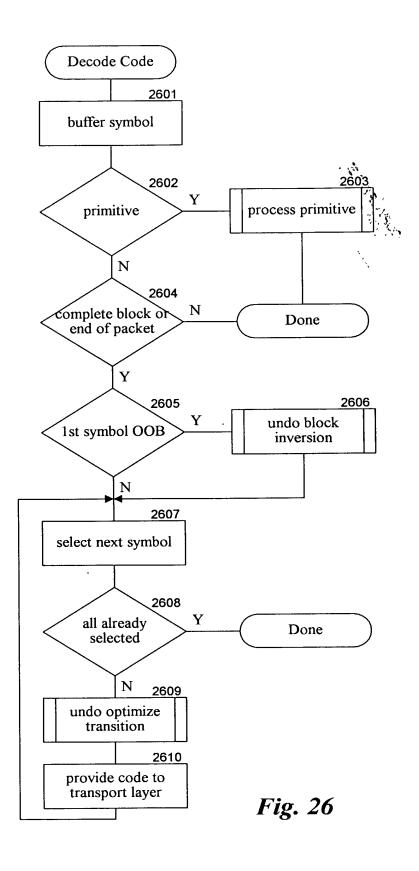


Fig. 25



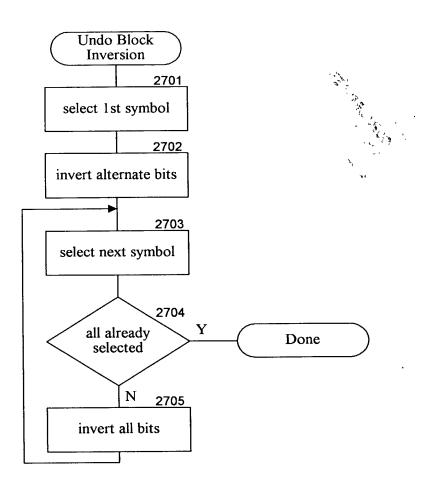


Fig. 27

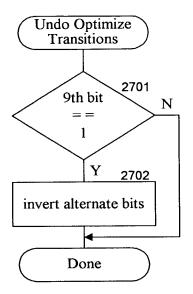


Fig. 28

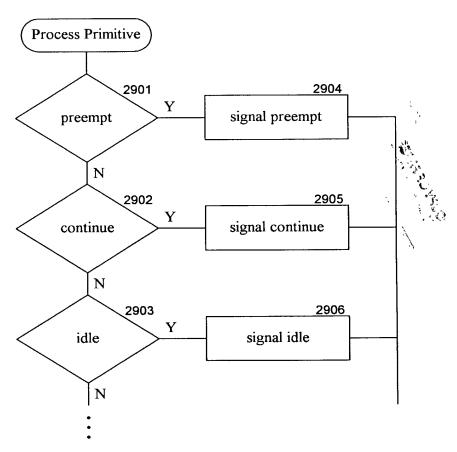
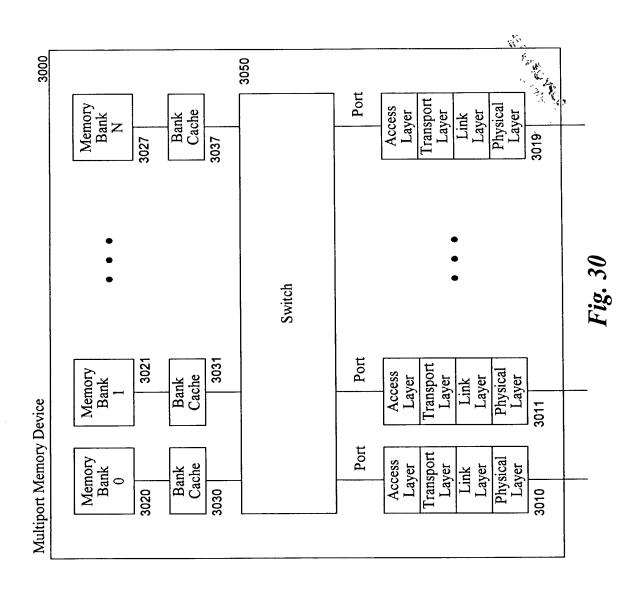
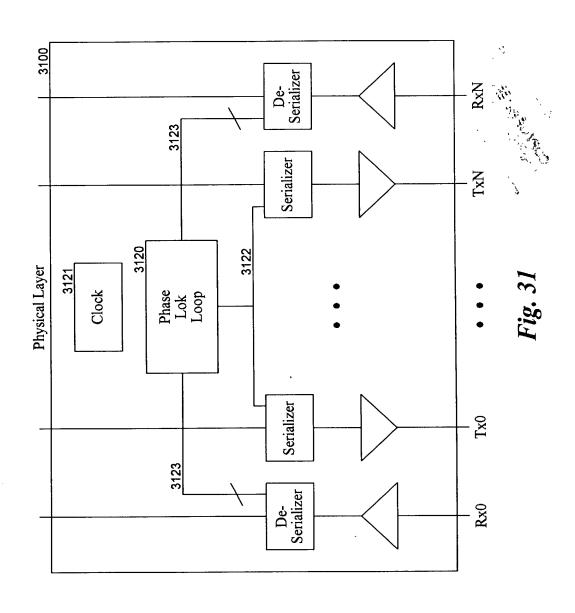


Fig. 29





Output Queue 3202	Data	110			1011	
	Valid Port	3			3	• • •
	Valid	1	0	0	1	
3201	Data		101	1110		
Input Queue	Address	1000	4000	1000	2000	
	R/W	R	M	M	R	• • •
	Port	3	4	3	3	

Fig. 32

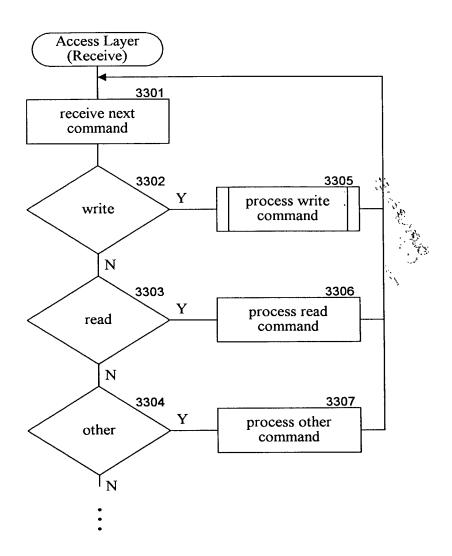


Fig. 33

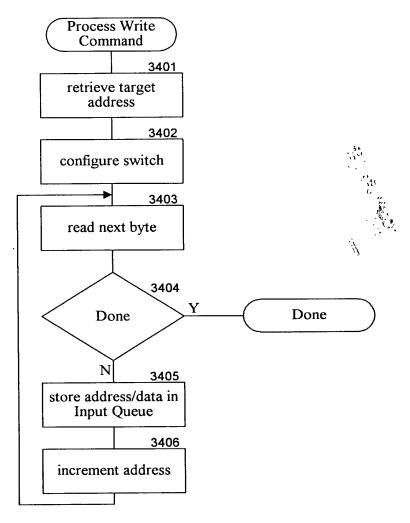
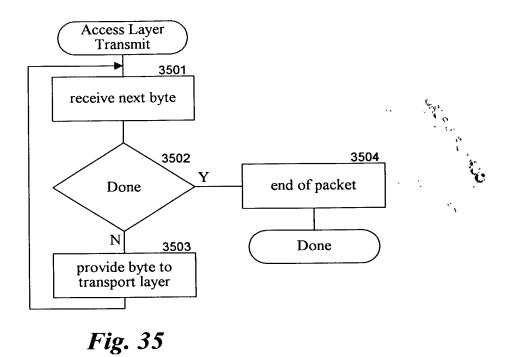
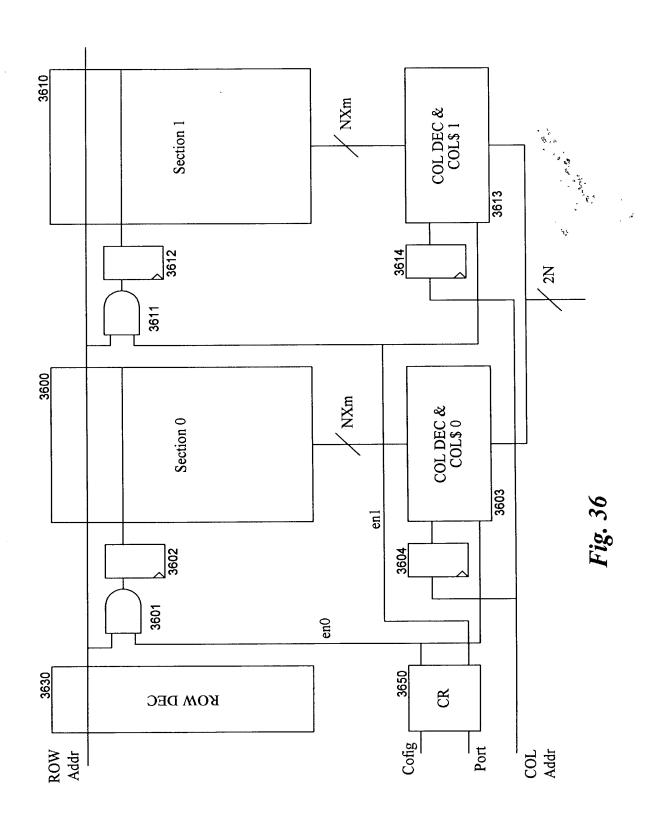


Fig. 34





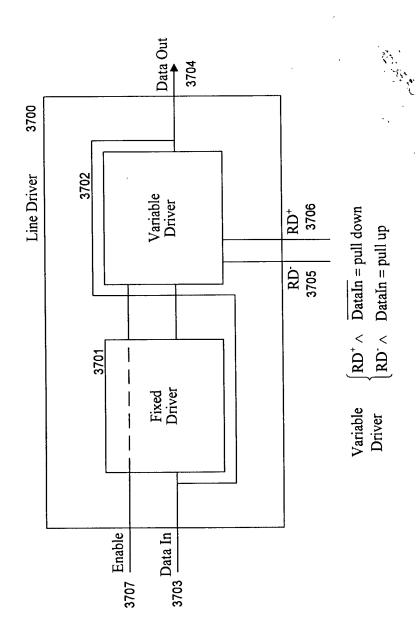
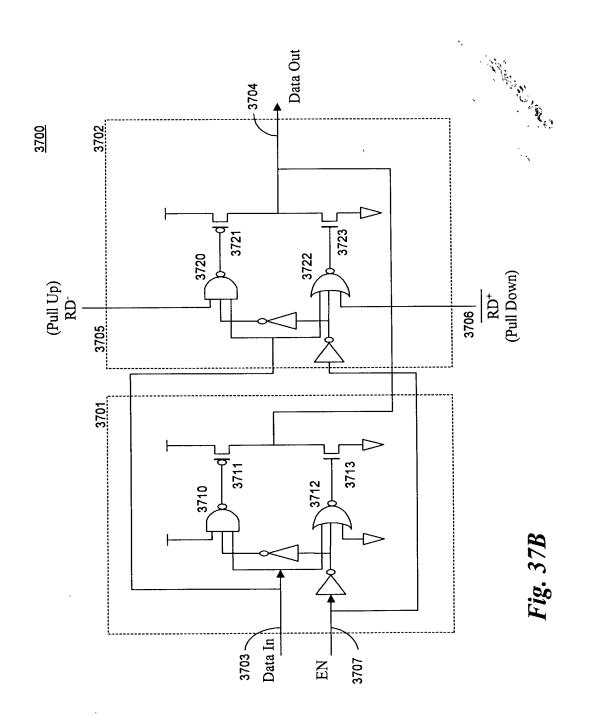
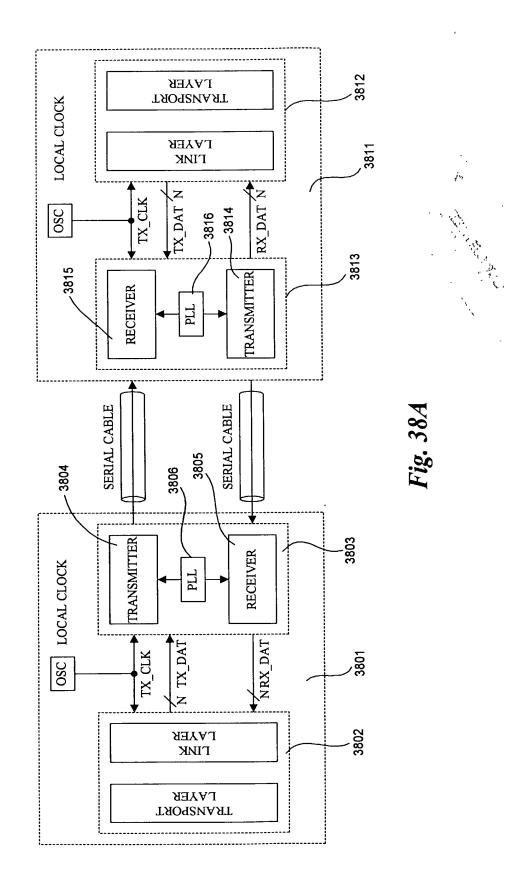
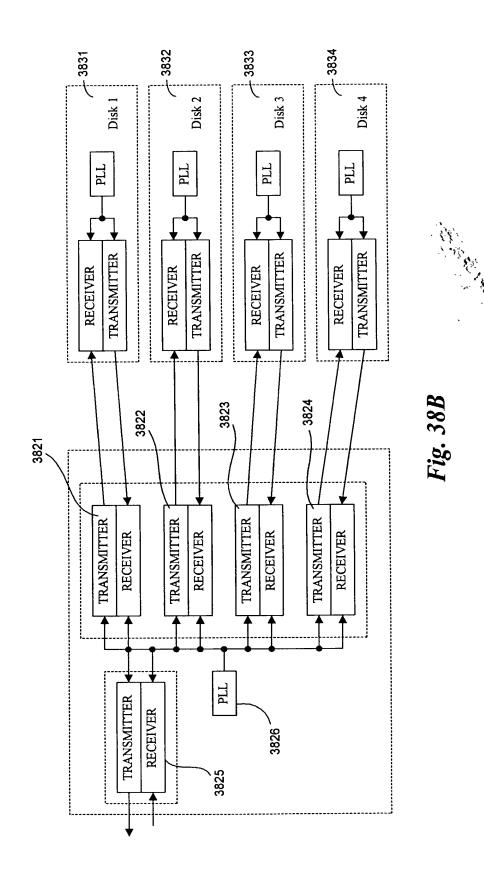
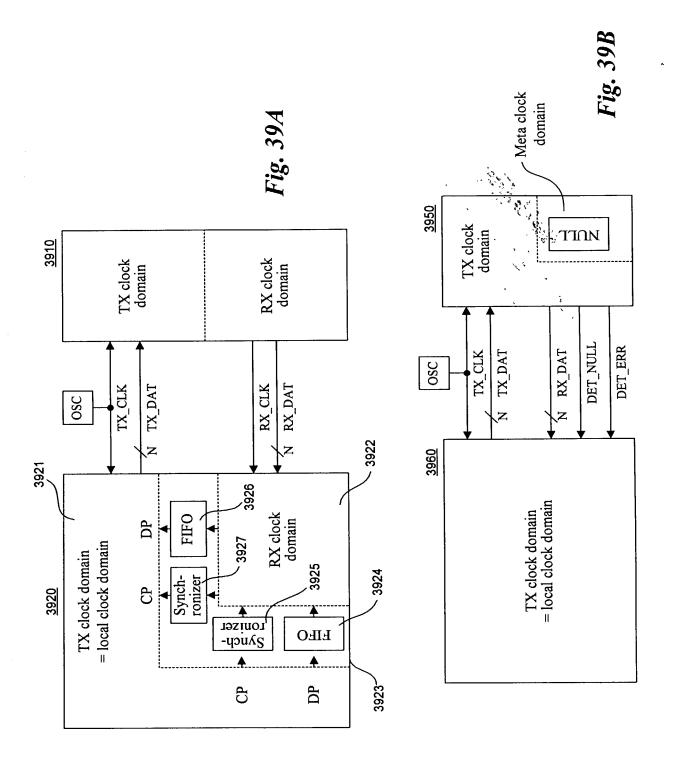


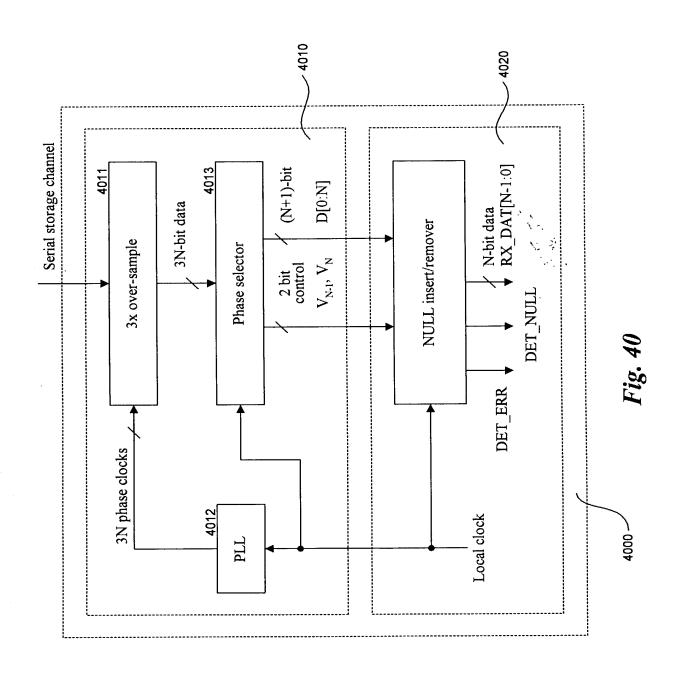
Fig. 374

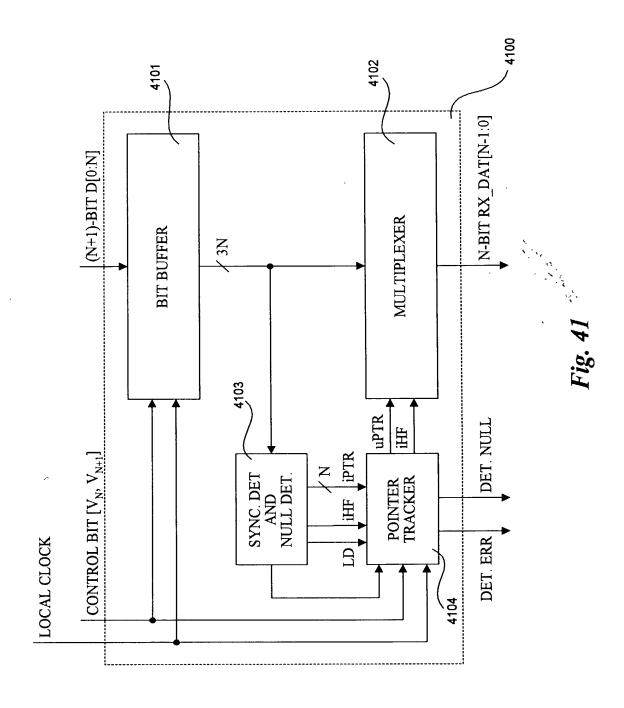


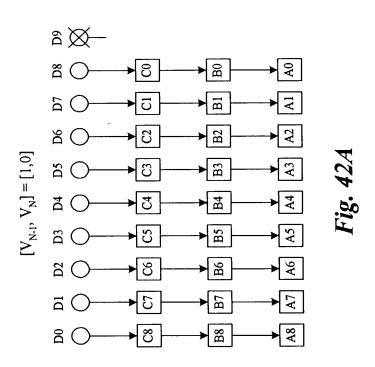


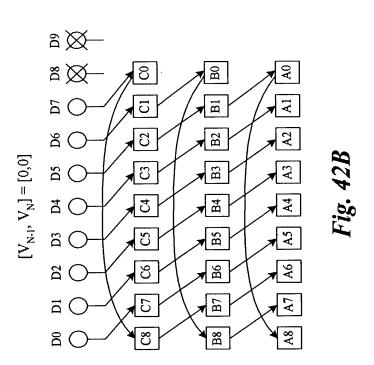


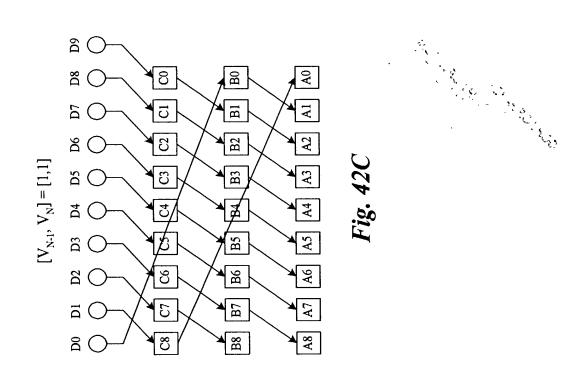


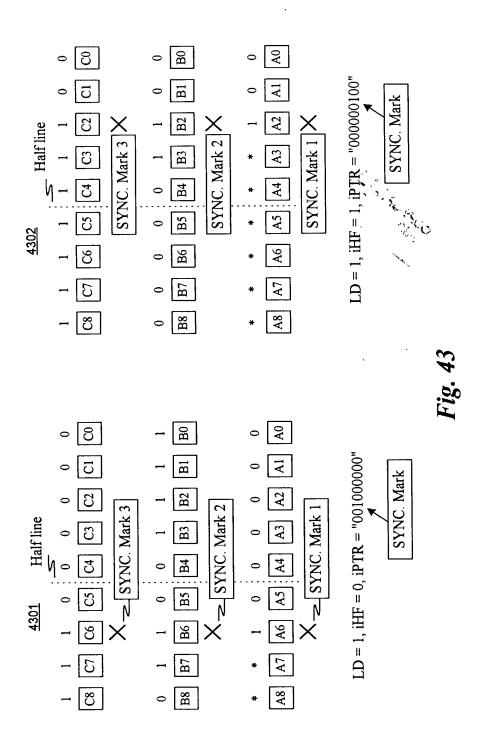


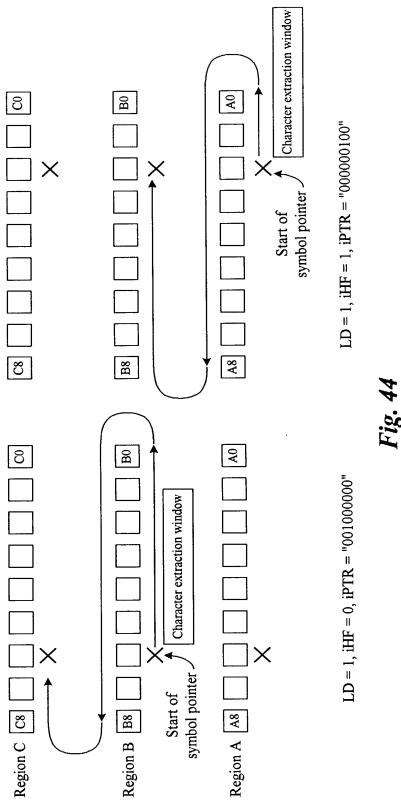




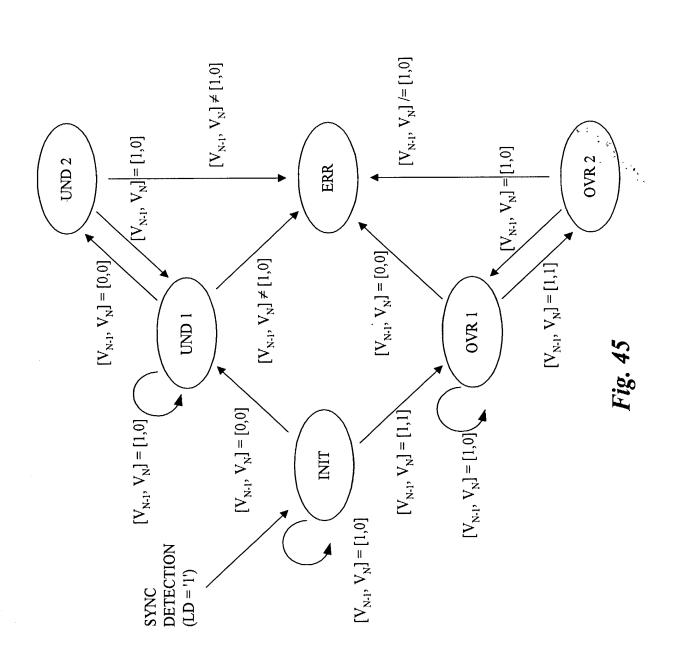








. To



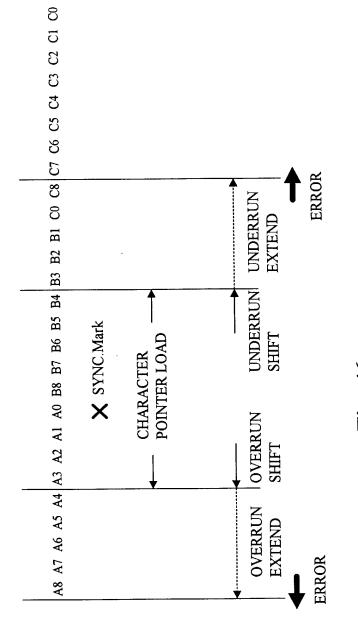
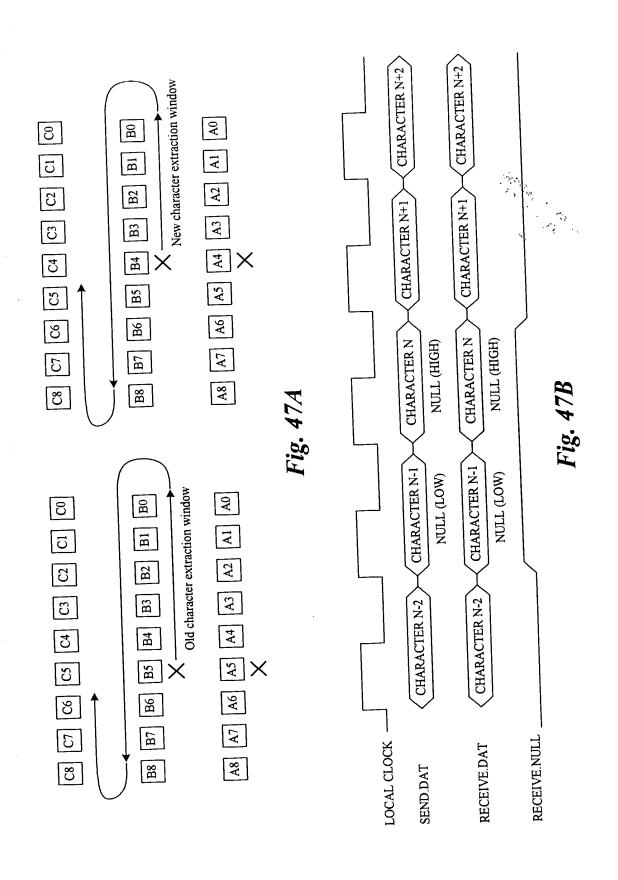


Fig. 46



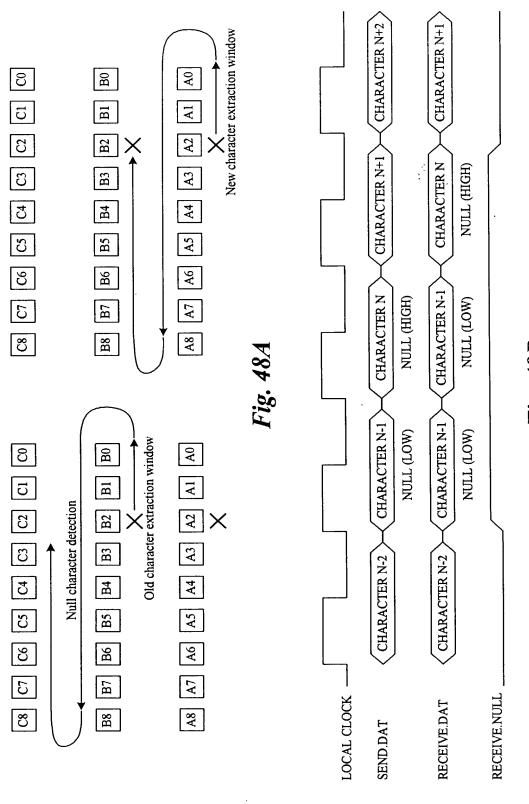
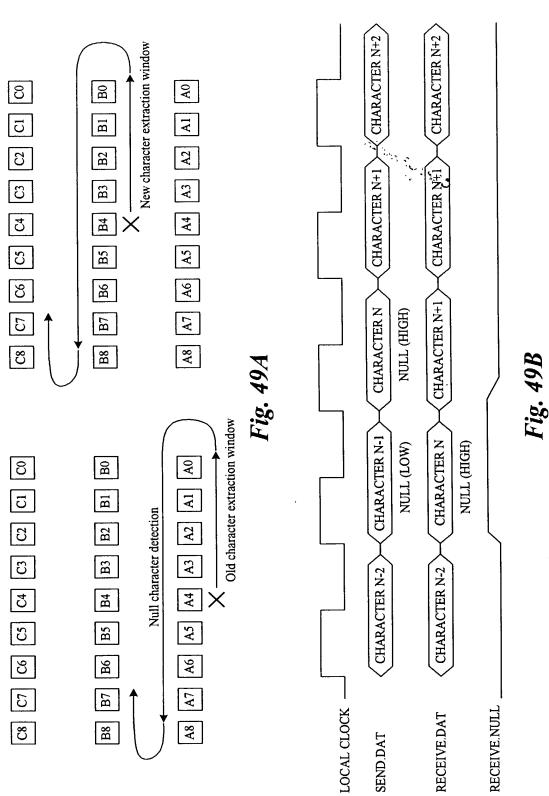


Fig. 48B



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